IN THE CLAIMS

Please amend the currently pending claims as follows.

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method, comprising:

generating a primary interrupt queue head and a secondary interrupt queue head, the primary and secondary interrupt queue heads to represent an endpoint, the endpoint to represent a transaction ~~with~~ between a host and at least one remote device over a serial bus, wherein execution of the endpoint requires more than one frame, each frame comprising a plurality of micro-frames and one of the host and the remote device is one is a high-speed device and the other is at least one of a full-speed and a low-speed device;

initializing the primary and secondary interrupt queue heads; and

scheduling the primary and secondary interrupt queue heads, wherein the primary interrupt queue head is positioned in a first micro-frame and wherein the secondary interrupt queue head is positioned in a second micro-frame, the second micro-frame being immediately subsequent to the first micro-frame.

2. (Original) The method of claim 1, wherein the generating of the primary and secondary interrupt queue heads is done when the execution of the endpoint is

to begin in one of a third, fourth, or fifth micro-frame in the plurality of micro-frames.

3. (Cancelled)

4. (Previously presented) The method of claim 1, wherein the initializing of the primary and secondary interrupt queue heads further comprises:

initializing the primary interrupt queue head to perform one start split transaction; and

initializing the secondary interrupt queue head to perform two complete split transactions.

5. (Previously presented) The method of claim 1, wherein the initializing of the primary and secondary interrupt queue heads further comprises:

initializing the primary interrupt queue head to perform one start split transaction and one complete split transaction; and

initializing the secondary interrupt queue head to perform two complete split transactions.

6. (Previously presented) The method of claim 1, wherein the initializing of the primary and secondary interrupt queue heads further comprises:

initializing the primary interrupt queue head to perform one start split transaction and two complete split transactions; and

initializing the secondary interrupt queue head to perform one complete split transaction.

7. (Original) The method of claim 1, further comprising reinitializing the primary and secondary interrupt queue heads.

8. (Original) The method of claim 1, wherein the at least one remote device is a full-speed or low-speed device.

9. (Cancelled)

10. (Original) The method of claim 9, further comprising polling the secondary interrupt queue head to determine the status of the secondary interrupt queue head.

11. (Original) The method of claim 9, further comprising polling the primary interrupt queue head to determine the status of the primary interrupt queue head.

12. (Currently amended) A machine-readable medium that includes instructions, which when executed by a machine, causes the machine to perform a method, the method comprising:

generating a primary interrupt queue head and a secondary interrupt queue head, the primary and secondary interrupt queue heads to represent an endpoint,

the endpoint to represent a transaction ~~with~~ between a host and at least one remote device over a serial bus, wherein execution of the endpoint requires more than one frame, each frame comprising a plurality of micro-frames and one of the host and the remote device is one is a high-speed device and the other is at least one of a full-speed and a low-speed device;

initializing the primary and secondary interrupt queue heads; and

scheduling the primary and secondary interrupt queue heads, wherein the primary interrupt queue head is positioned in a first micro-frame and wherein the secondary interrupt queue head is positioned in a second micro-frame, the second micro-frame being immediately subsequent to the first micro-frame.

13. (Original) The machine-readable medium of claim 12, wherein the generating of the primary and secondary interrupt queue heads is done when the execution of the endpoint is to begin in one of a third, fourth, or fifth micro-frame in the plurality of micro-frames.

14. (Cancelled)

15. (Previously presented) The machine-readable medium of claim 12, wherein the initializing of the primary and secondary interrupt queue heads further comprises:

initializing the primary interrupt queue head to perform one start split transaction; and

initializing the secondary interrupt queue head to perform two complete split transactions.

16. (Previously presented) The machine-readable medium of claim 12, wherein the initializing of the primary and secondary interrupt queue heads further comprises:

initializing the primary interrupt queue head to perform one start split transaction and one complete split transaction; and

initializing the secondary interrupt queue head to perform two complete split transactions.

17. (Previously presented) The machine-readable medium of claim 12, wherein the initializing of the primary and secondary interrupt queue heads further comprises:

initializing the primary interrupt queue head to perform one start split transaction and two complete split transactions; and

initializing the secondary interrupt queue head to perform one complete split transaction.

18. (Original) The machine-readable medium of claim 12, further comprising reinitializing the primary and secondary interrupt queue heads.

19. (Original) The machine-readable medium of claim 12, wherein the at least one remote device is a full-speed or low-speed device.

20. (Cancelled)

21. (Currently amended) The machine-readable medium of ~~claim 20~~ claim 12, further comprising polling the secondary interrupt queue head to determine the status of the secondary interrupt queue head.

22. (Currently amended) The machine-readable medium of ~~claim 20~~ claim 12, further comprising polling the primary interrupt queue head to determine the status of the primary interrupt queue head.

23. (Currently amended) An apparatus, comprising:

a high-speed serial bus;

a full-/low-speed serial bus;

a hub, comprising:

a transaction translator unit, coupled with the high-speed serial bus and the full-/low-speed serial bus, to translate bits of data associated with an endpoint between a transfer rate associated with the high-speed serial bus and a transfer rate associated with the full-/low-speed serial bus;

a high-speed host, comprising:

a host controller driver unit to generate, initialize, and schedule a primary interrupt queue head and a secondary interrupt queue head, the primary and secondary interrupt queue heads to represent the endpoint, the endpoint representing a transaction ~~with~~ between the host and at the least one remote device, wherein execution of the endpoint requires more than one frame, each frame comprising a plurality of micro-frames;

a host controller unit, coupled with the high-speed serial bus and the host controller driver unit, to transmit the bits of data associated with the endpoint to and receive the bits of data associated with the endpoint from at least one remote device; and

the at least one remote device, coupled with the full-/low-speed serial bus, to transmit bits of data associated with the endpoint to and receive bits of data associated with the endpoint from the host controller unit.

24. (Previously presented) The apparatus of claim 23, wherein the host controller driver unit is to schedule the primary and secondary interrupt queue heads such that the primary queue head is positioned in a first micro-frame and such that the secondary interrupt queue head is positioned in a second micro-frame, the second micro-frame being immediately subsequent to the first micro-frame.

25. (Original) The apparatus of claim 23, wherein the host controller driver unit is to generate the primary and secondary interrupt queue heads when the

execution of the endpoint is to begin in one of a third, fourth, or fifth micro-frame in the plurality of micro-frames.

26. (Previously presented) The apparatus of claim 23, wherein the host further comprises an enhanced host controller interface unit, which includes the host controller unit, the enhanced host controller interface unit to provide an interface between the host controller unit and the host controller driver unit.

27. (Cancelled)

28. (Currently amended) A system, comprising:

a high-speed signaling environment;

a full-/low speed signaling environment;

a hub, wherein the hub is located within the high-speed signaling environment and the full-/low speed signaling environment, to translate bits of data associated with an endpoint between a transfer rate associated with the high-speed signaling environment and a transfer rate associated with the full-/low-speed signaling environment;

a high-speed host, located within the high-speed signaling environment, coupled with the hub, to transmit bits of data associated with an endpoint to and receive bits of data associated with the endpoint from at least one full-/low speed remote device, and to generate, initialize, and schedule a primary interrupt queue head and a secondary interrupt queue head, the primary and secondary interrupt

queue heads to represent the endpoint, the endpoint representing a transaction ~~with~~ between the host and at the least one remote device, wherein execution of the endpoint requires more than one frame, each frame comprising a plurality of micro-frames; and

the at least one full-/low speed remote device, coupled with the hub, to transmit bits of data to and receive bits of data from the host, wherein the at least one remote device is located within the full-/low-speed signaling environment.

29. (Previously presented) The system of claim 28, wherein the host is to schedule the primary and secondary interrupt queue heads such that the primary interrupt queue head is positioned in a first micro-frame and such that the secondary interrupt queue head is positioned in a second micro-frame, the second micro-frame being immediately subsequent to the first frame.

30. (Original) The system of claim 28, wherein the host is to generate the primary and secondary interrupt queue heads when the execution of the endpoint is to begin in one of a third, fourth, or fifth micro-frame in the plurality of micro-frames.